PARADIGM™ WORKS

Formal Verification Techniques

Saeed Coates

Equivalence Checking

Chrysalis

- RTL-to-netlist comparisons
- Used to verify that the design has not changed functionally from synthesis all the way through tapeout

Property Checking

Beyond Equivalence Checking

- **Equivalence Checking**
  - Existing bugs can pass through undetected
- **Property Checking**
  - Exhaustively verifies a design and captures bugs early in the development process

Exhaustive Verification

- No test vectors or testbenches
- Steps through all combinations at the design's inputs
- Overcomes the code coverage limitations of simulations
- Minimal time to cover a large portion of a design's state space

Standard Checks

- **Semantic inconsistencies**
  - Synopsys full/parallel case directives
  - Range overflow
- **Structural inconsistencies**
  - Bus contention and floating bus issues
  - Stuck tri-state enables
- **Assertion checks and other user-defined checks**

Time Consuming Simulations

100 T

100 B

Simulation Cycles

100 M

1995 · 2001 · 2007

1 M · 10 M · 100 M

Gates
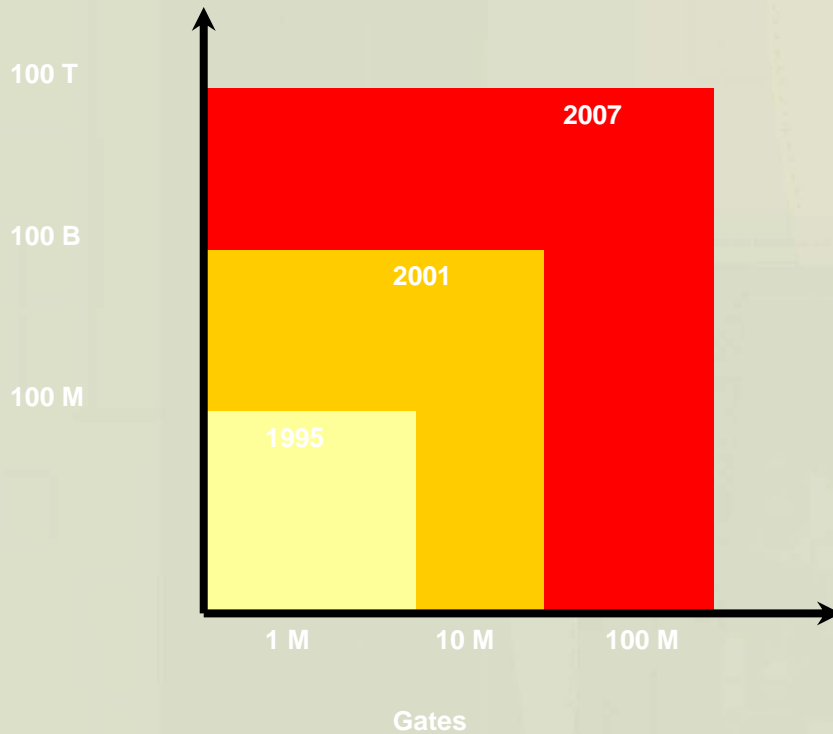
Assertion-Based Verification

Assertion

- A statement that checks that a property holds true
- Complete checkers/monitors can be built from assertions

Assertion Property

- A fundamental design characteristic that must hold true during operation
- Defined in an HDL or an FPL
- Stored in an Assertion Property Library

Benefits of Assertions

- Simulates with the design

- Reduces debug time by pinpointing bugs

- Eases IP integration for customers

- Most powerful when combined with a formal property checker

Adding Assertions

> Around multiply instantiated blocks (eg. shipping 3rd party IP/reusable designs)

> Inline w/ code (eg. ensuring that a fundamental condition is always met)

> At the system level (eg. bus protocol monitors)

> At block boundaries (eg. ensuring designers adhere to a negotiated interface between blocks built by different designers)

FPLs

- Accellera proposing IBM's FPL called "Sugar" for IEEE standardization
- Synopsys' OVA (Open Vera Assertion)
- 0-In Design Automation's 0-In Check Library

OVL

Open Verification Library

Free download at:

http://www.verificationlib.org