



Synopsys Users Group
SILICON VALLEY 2012

Integrating *DesignWare USB3 Device Controller IP* Into a **UVM-based** Testbench

Ning Guo
Paradigm Works



Background

- ❑ Collaboration project between Paradigm Works and Synopsys
- ❑ A plug-n-play type UVM environment for **Any** USB3 Device DUT verification
 - Environment is built with *Synopsys Discovery Verification IPs*
 - ❖ Discovery USB3 VIP, Discovery AMBA VIP
 - DUT for the environment development is **Synopsys DesignWare USB3 Controller IP (DWC_USB3)**
 - ❖ Pre-verified IP
- ❑ Available as part of Synopsys Discovery USB3 VIP Library

Outline

- ❑ DWC_USB3 Device IP integration Process
 - Integrate into the Testbench Module
 - Integrate into the UVM Environment

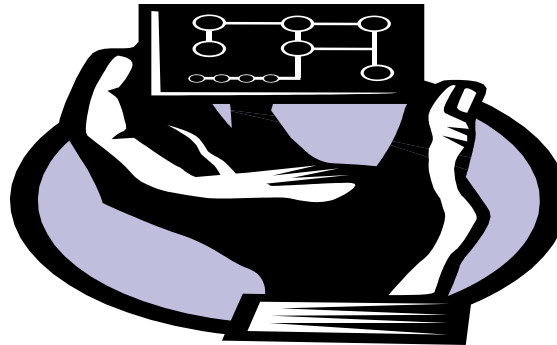
- ❑ DWC_USB3 Device IP Configuration Flow
- ❑ DWC_USB3 Device IP Operation Flow

- ❑ Plug-n-Play capability of the UVM Environment

DWC_USB3 Controller IP



Synopsys Users Group
SILICON VALLEY 2012



USB3 Device Controller

USB3 Host Controller

USB3 Dual-Role Device Controller

USB3 Hub Controller



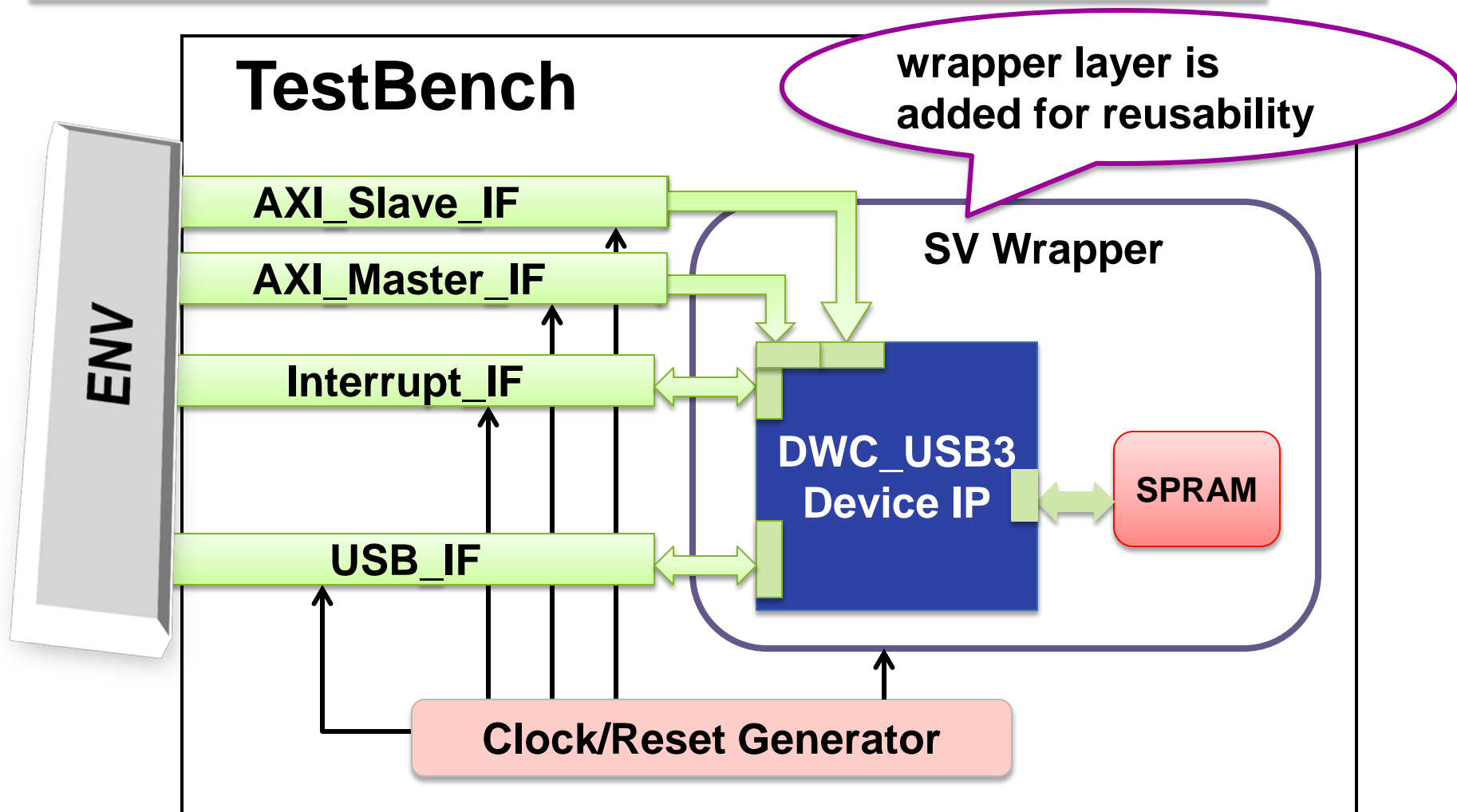
Outline

- ❑ DWC_USB3 Device IP integration Process
 - Integrate into the Testbench Module
 - Integrate into the UVM Environment

- ❑ DWC_USB3 Device IP Configuration Flow
- ❑ DWC_USB3 Device IP Operation Flow

- ❑ Plug-n-Play capability of the UVM Environment

Integration - Module Level



Integration – Module Level (2)

```
module DWC_usb3_sv_wrapper (
```

```
  input clk,
```

```
  svt_usb_if usb
```

```
  svt_usb_if usb_s
```

```
  rtl_dut_intr_if dut_intr_if,
```

```
  svt_axi_master_if axi_master_if,
```

```
  svt_axi_slave_if axi_slave_i
```

```
);
```

```
DWC_usb3 dut(.TxData(dut_pipe3_TxData),.RxValid(dut_pipe3_RxValid),...);
```

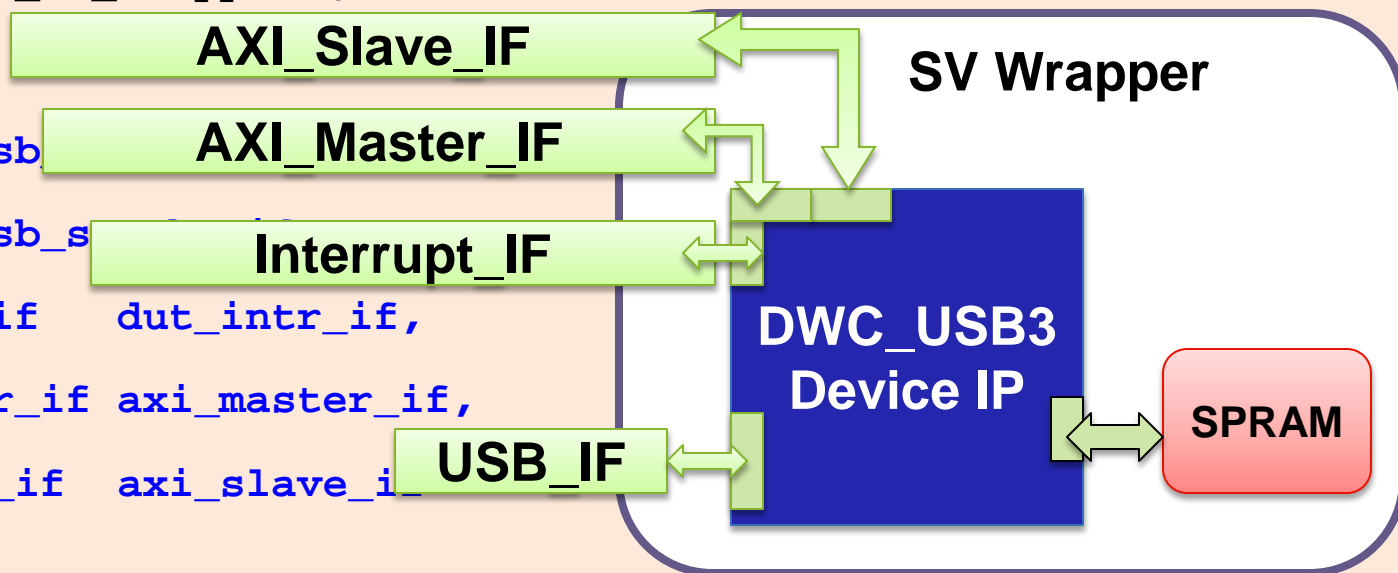
```
spram_model#(`DWC_USB3_RAM0_DEPTH,32) ram0(
```

```
  .clk(clk), .rst_n(tb_vcc_reset_n),
```

```
  .cs_n(dut_ram0_p1_ce_n),.wr_n(dut_ram0_p1_wr_n),
```

```
  .rw_addr(dut_ram0_p1_addr),.data_in(dut_ram0_p1_wdata),
```

```
  .data_out(dut_ram0_p1_rdata));
```



```
Data;  
Valid;
```

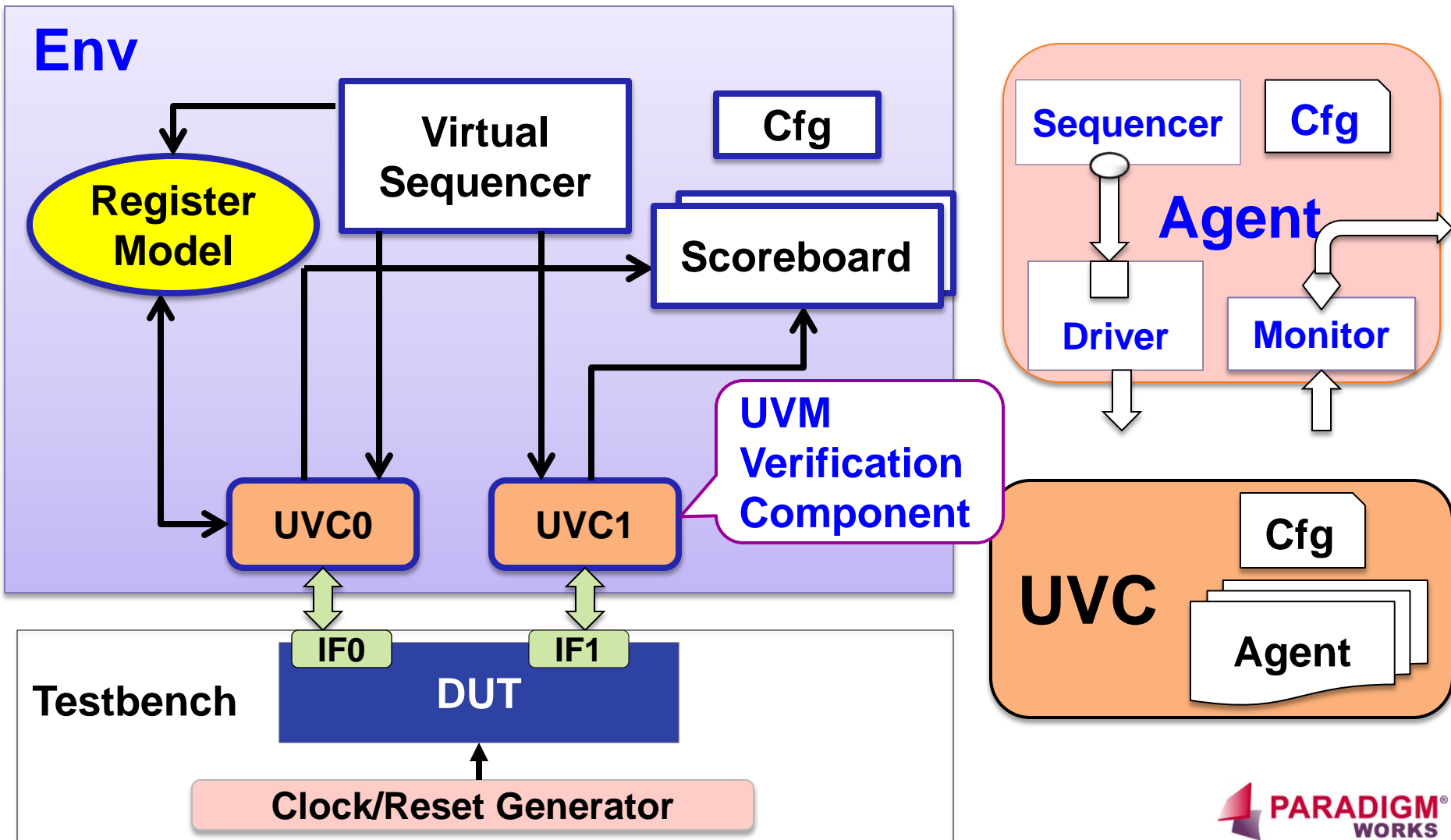
Outline

- ❑ DWC_USB3 Device IP integration Process
 - Integrate into the Testbench Module
 - Integrate into the UVM Environment

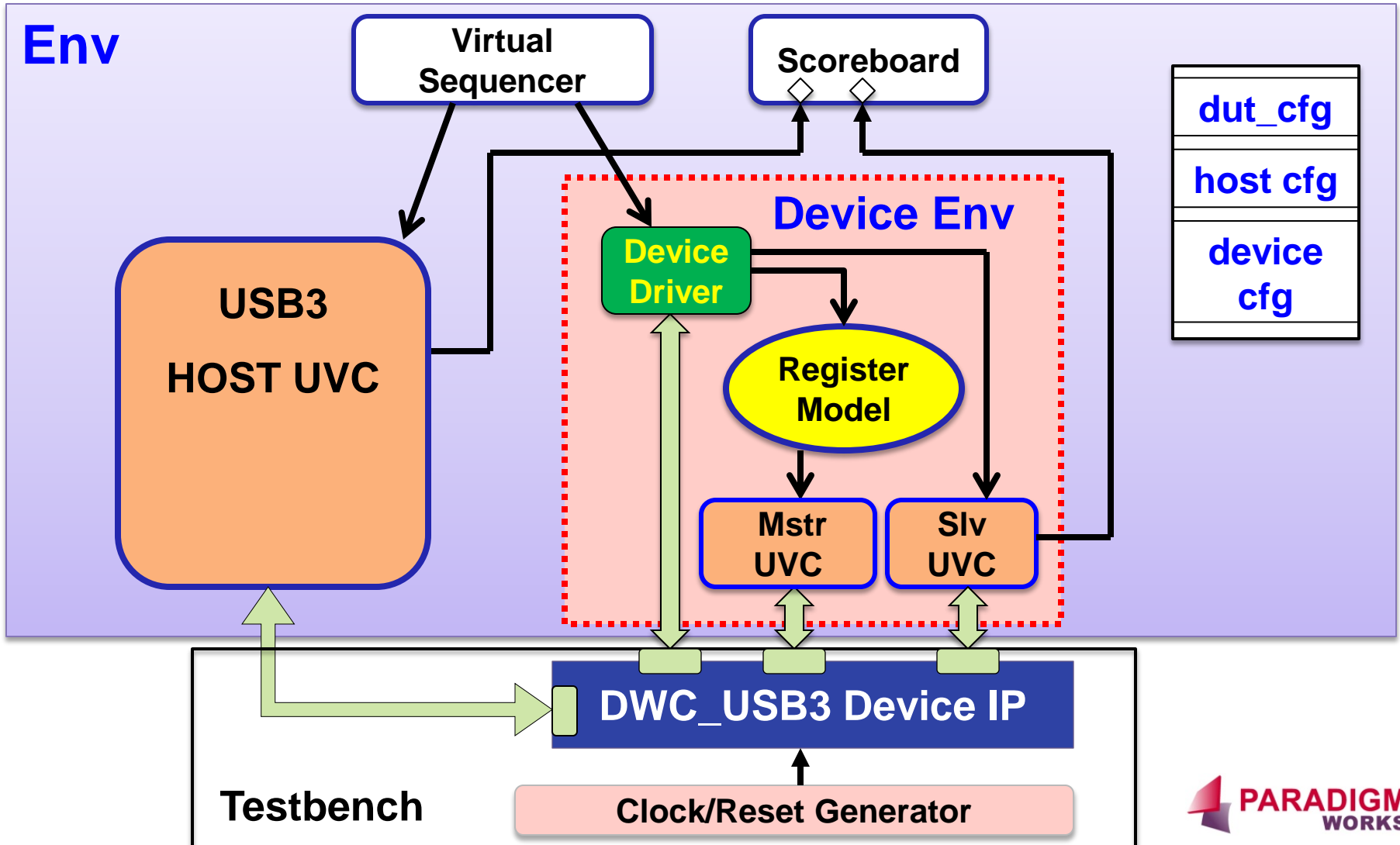
- ❑ DWC_USB3 Device IP Configuration Flow
- ❑ DWC_USB3 Device IP Operation Flow

- ❑ Plug-n-Play capability of the UVM Environment

Integration - UVM Env



Integration – DWC_USB3 Device Verification Env



Outline

- ❑ DWC_USB3 Device IP integration Process
 - Integrate into the Testbench Module
 - Integrate into the UVM Environment

- ❑ DWC_USB3 Device IP Configuration Flow
- ❑ DWC_USB3 Device IP Operation Flow

- ❑ Plug-n-Play capability of the UVM Environment

Configuration - Device Driver

Device Driver extends uvm_component

`build_phase()`

`connect_phase()`

```

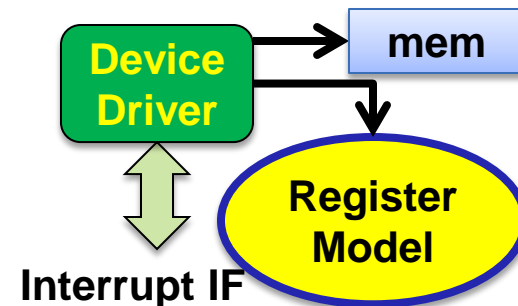
configure_phase() {
  // Start Interrupt Service
  // Do Power On Reset sequence
  // Do USB Reset sequence
  // Do Connect Done sequence
}

```

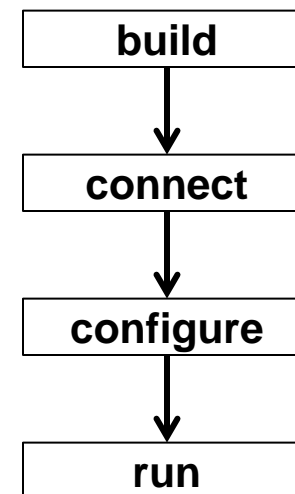
```

run_phase() {
  // Get device response from sequencer
  // Write transfer info to memory
  // Issue transfer and wait for it to complete
}

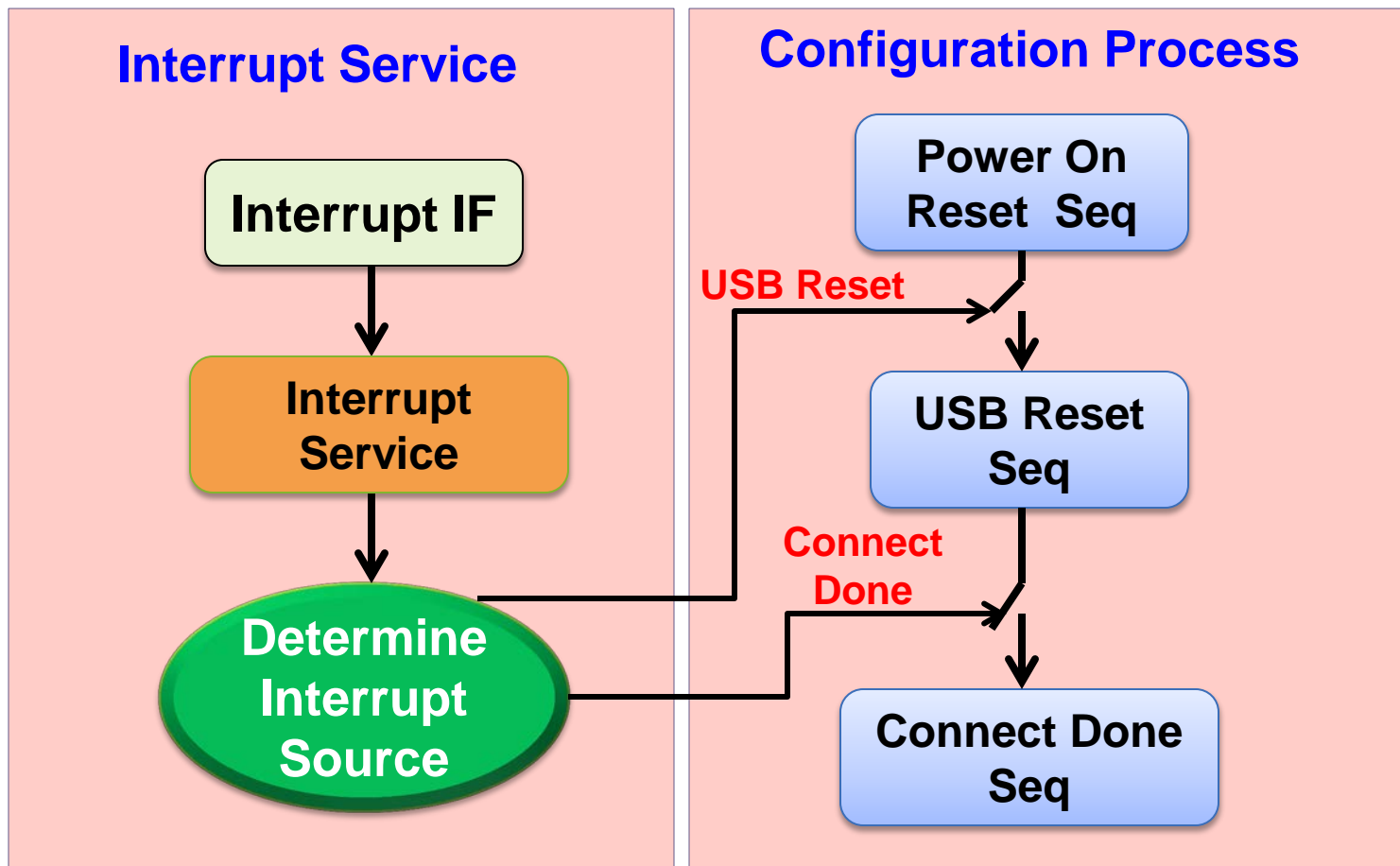
```



UVM Phasing



Configuration – `configure_phase`



Outline

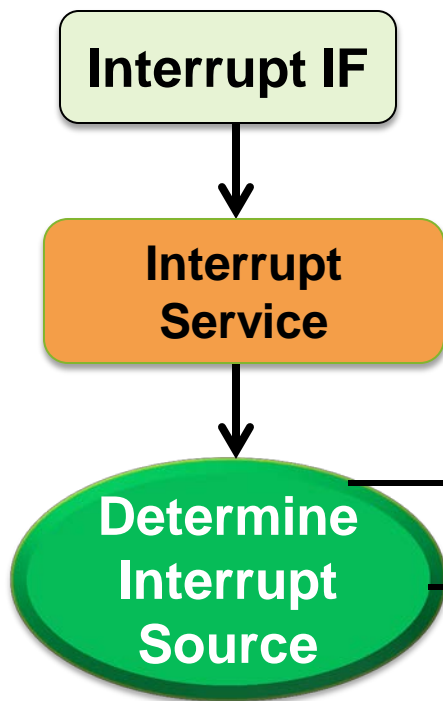
- ❑ DWC_USB3 Device IP integration Process
 - Integrate into the Testbench Module
 - Integrate into the UVM Environment

- ❑ DWC_USB3 Device IP Configuration Flow
- ❑ DWC_USB3 Device IP Operation Flow

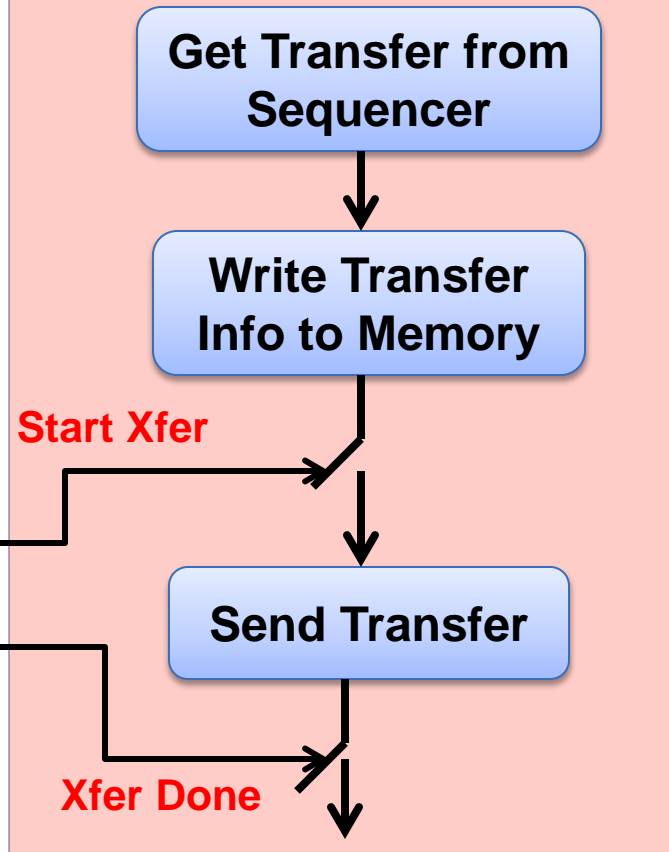
- ❑ Plug-n-Play capability of the UVM Environment

Operation – run_phase

Interrupt Service



Data Transfer Process



Outline

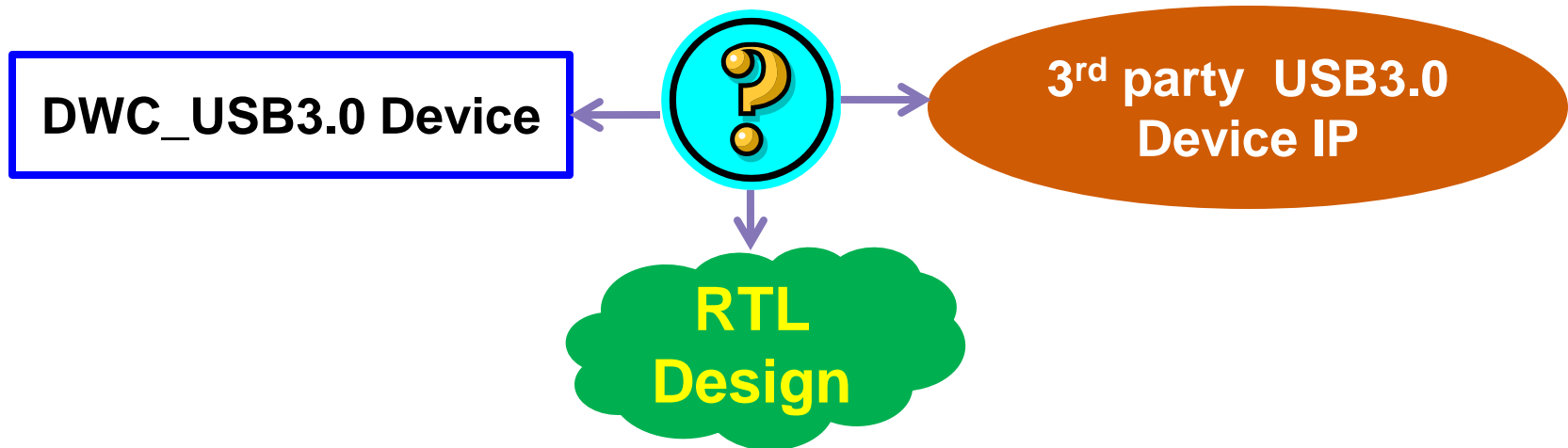
- ❑ DWC_USB3 Device IP integration Process
 - Integrate into the Testbench Module
 - Integrate into the UVM Environment

- ❑ DWC_USB3 Device IP Configuration Flow
- ❑ DWC_USB3 Device IP Operation Flow

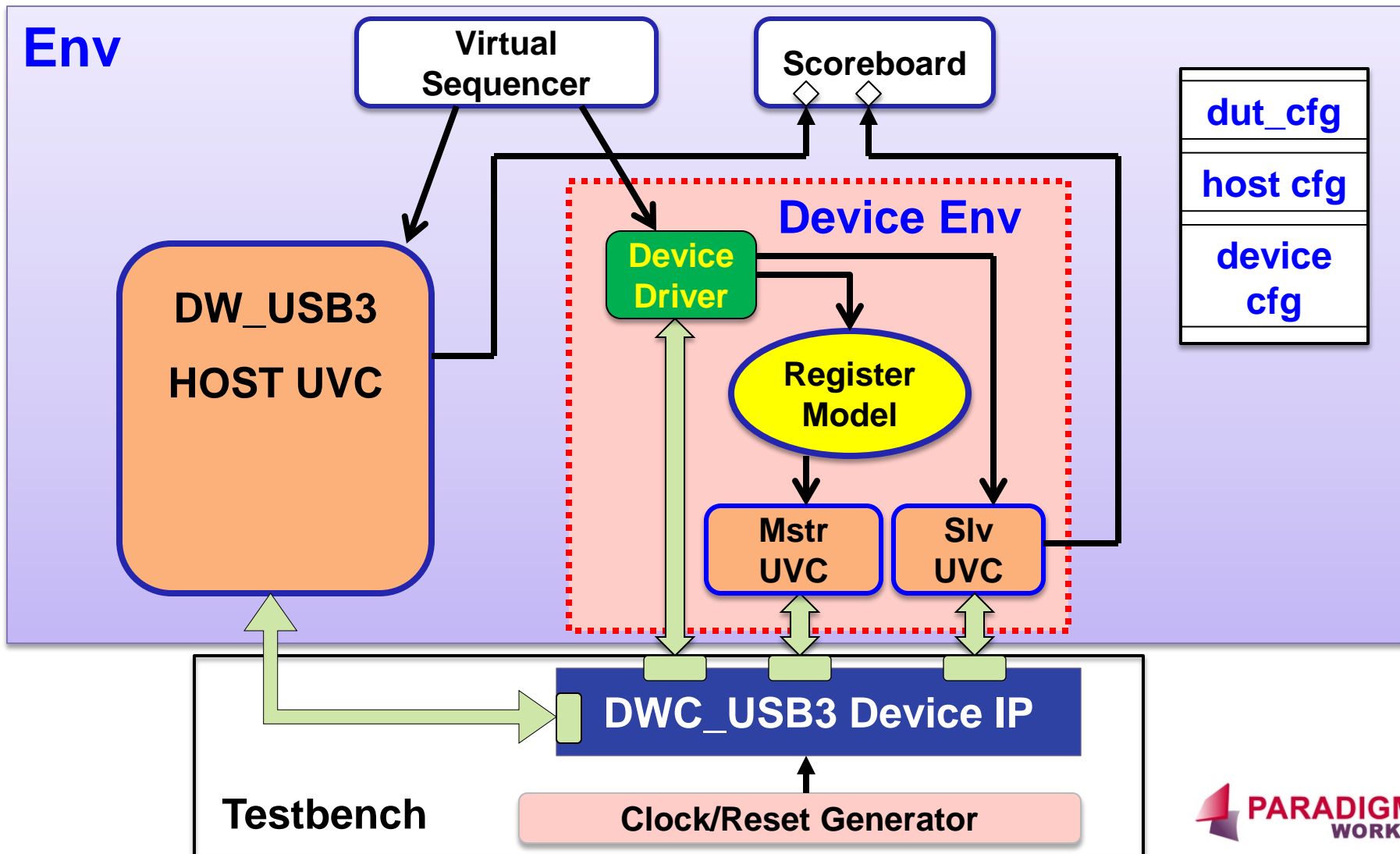
- ❑ Plug-n-Play capability of the UVM Environment

Reuse

□ What is your Device DUT?

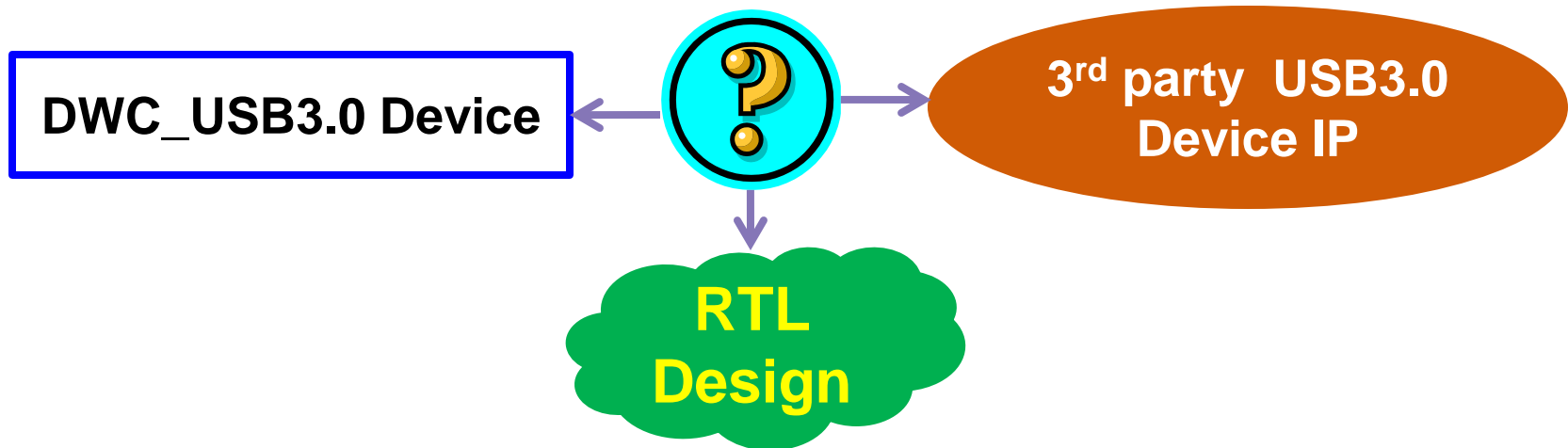


Reuse – DWC_USB3 Variation

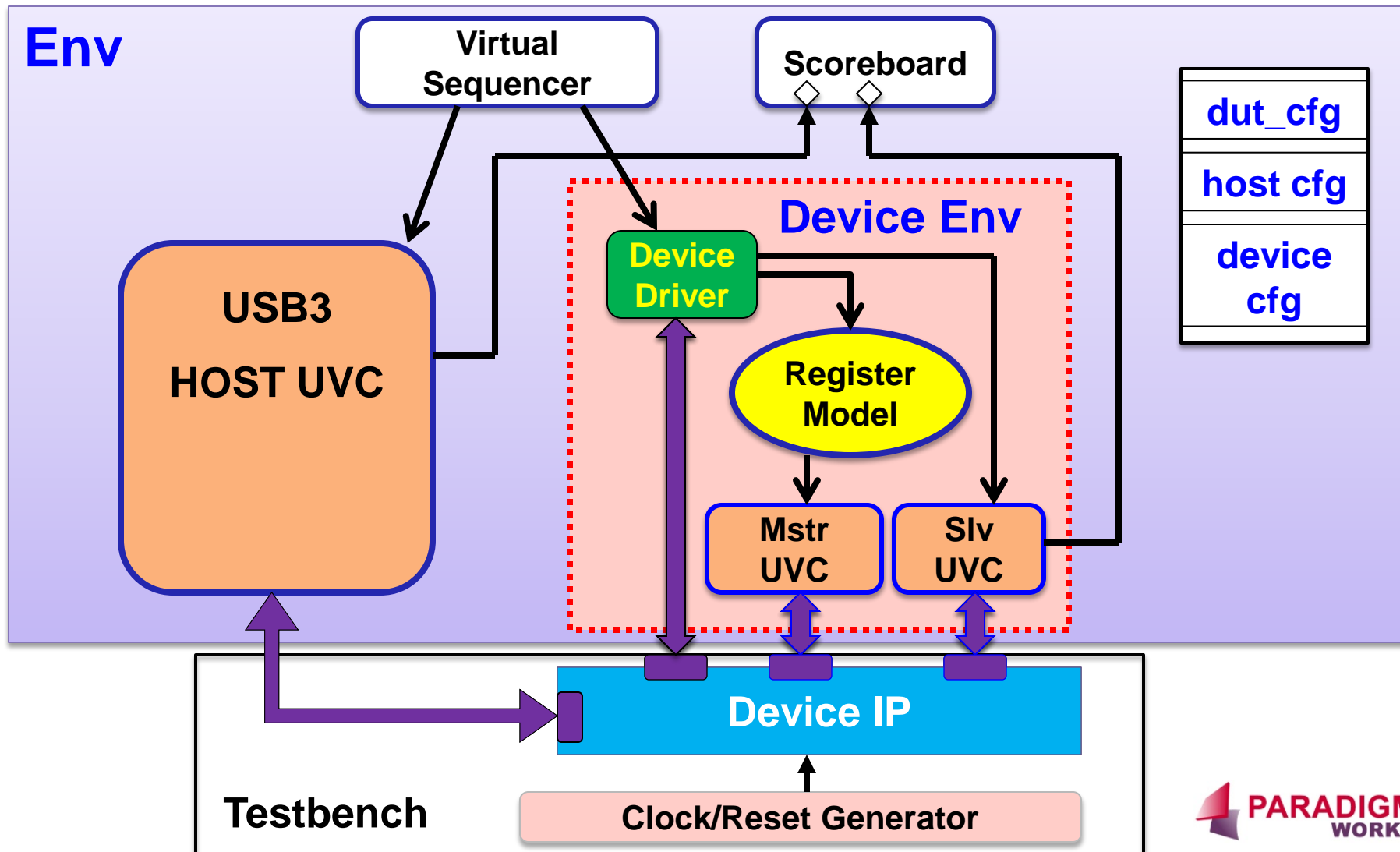


Reuse

□ What is your Device DUT?



Reuse – 3rd Party IP or RTL Design



Configuration - Device Driver

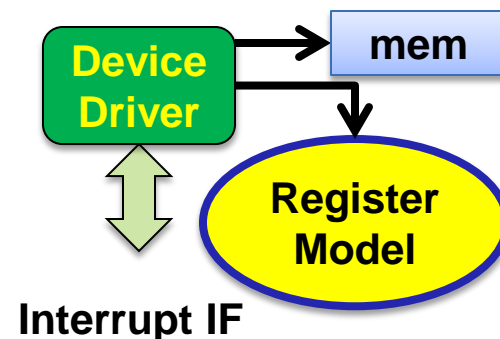
Device Driver extends uvm_component

`build_phase()`

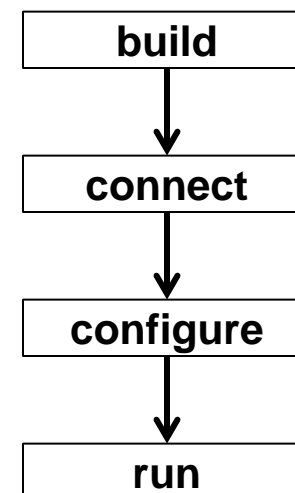
`connect_phase()`

```
configure_phase() {
  // Start Interrupt Service
  // Do Power On Reset sequence
  // Do USB Reset sequence
  // Do Connect Done sequence
}
```

```
run_phase() {
  // Get device response from sequencer
  // Write transfer info to memory
  // Issue transfer and wait for it to complete
}
```



UVM Phasing



Summary

- ❑ Plug-n-Play UVM environment for USB3 Device DUT Verification
- ❑ DWC_USB3 Device IP to help develop the environment
- ❑ Env and pre-defined tests (Test Suite) will be part of Synopsys Discovery USB3 VIP Library (Availability TBD)
- ❑ Currently Available
 - DesignWare USB3 Controller IP (DWC_USB3)
 - Discovery AMBA VIP
 - Discovery USB VIP



Synopsys Users Group
SILICON VALLEY 2012

Thank You !

