



Frame Transaction

Application Note

Revision 1.0

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1 Overview

Many verification teams today are challenged by the need to generate complicated traffic patterns with stacked protocols such as Ethernet in constrained random testbenches. Building up stacked protocols randomly, whilst at the same time enabling fine grained control over any of the protocol fields is a non-trivial task.

The VerificationWorks™ Frame Transaction class is a robust transaction class that enables the rapid creation and control of such protocols. It generates high level frames (or protocol stacks) that can be packed or unpacked to or from a lists of bytes (or bits), respectively. By default, the Frame Transaction class processes Ethernet encapsulated packets out-of-the-box, but can be adopted to create patterns for any stacked protocol. Examples of Ethernet encapsulation are MAC->IP->UDP and MAC-VLAN TAG->IP->TCP->PAYLOAD.

An architectural drawing of the Frame Transaction Class is shown below in Figure 1-1.

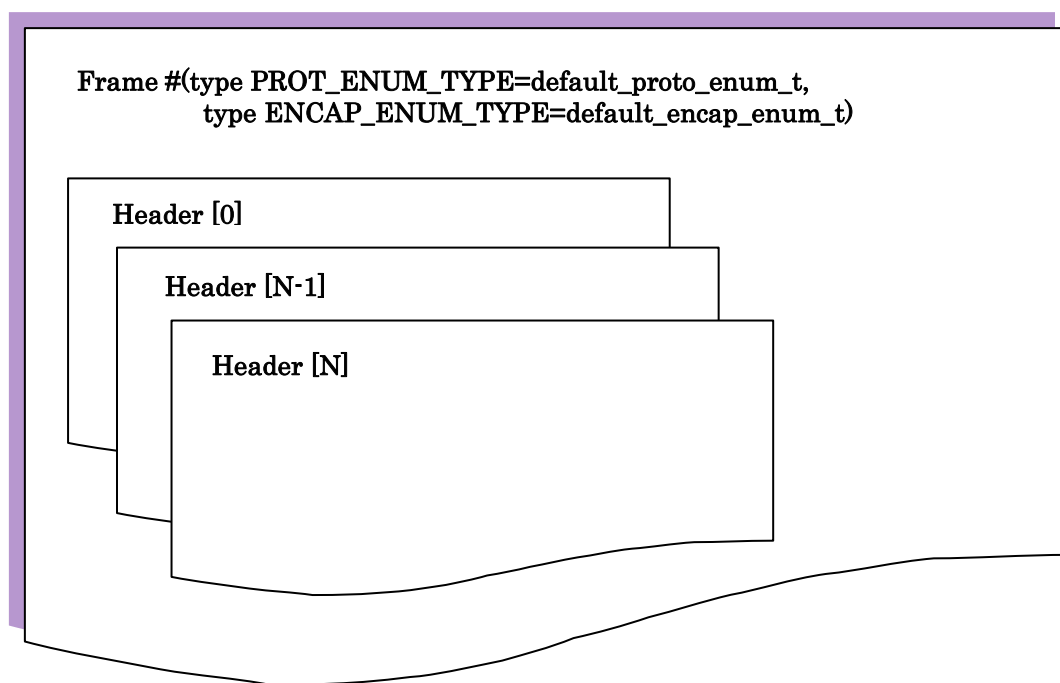


Figure 1-1: Frame Transaction Class

The frame class encapsulates "encapsulation schemes" and is a container for N number of "protocol header class instances". The frame class allows for users to use SystemVerilog in-line constraints to control encapsulation schemes along with modifying any field located inside the protocol header. The randomization of the encapsulation and all headers fields occurs inside a single UVM randomize call.

Summary of Frame Transaction features:

- Randomizes protocol headers and encapsulations
 - Default Supported Protocols
 - Preamble
 - Layer 2

- MAC
- 1 or more VLAN
- Ethernet II (Type encode)
- SNAP/LLC
- Layer 3
 - IPv4/IPv6
 - ARP/RARP
- Layer 4
 - TCP
 - UDP
 - ICMP
 - ICMPv6
 - IGMP
- Protocols include header/payload/trailer fields
- Users can add new protocols
- Encapsulation
 - Supports canned predefined "encapsulation" schemes
 - i.e. MAC->IPv4->TCP->Raw Payload
 - Users can add new "encapsulation" schemes
- Generation
 - Generates a frames class structure using SystemVerilog random/constraint technology
 - Users can control "encapsulations" using SystemVerilog constraints or in-line random constraints
 - i.e. MAC->IPv4->TCP->Raw Payload, MAC->2 VLANs->Raw Payload
 - Users can add new "encapsulation" schemes
 - Users can control the values of any field within a specific header/protocol using SystemVerilog constraints or in-line random constraints
 - Users may extend protocol classes in order to constrain fields to values that match specific application requirements
 - Automatically calculates header/trailer CRC/ FCS / Checksums during. These fields live in the "protocol" classes
 - Payloads
 - Payloads are included in "protocol" classes.
 - Payloads are controllable
- Pack/unpack
 - Packs from a frames class based protocol structure into a list of bits or bytes

- Unpacks a list of bits or bytes into a frame class based protocol structure
- Uses standardized UVM Packer and UVM Unpacker
- Compare
 - Uses standard UVM compare
 - We will likely override the do_compare functionality due to the complications of Ethernet
- Dumps out a format that can be read directly into Wireshark

2 Company Background

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